

**METHOD AND APPARATUS FOR SEARCHING TIME-DIVISION
MULTIPLEXED SYNCHRONIZATION SEQUENCES**

ABSTRACT OF THE DISCLOSURE

- [00050]** In a real-time mode, a clock signal of a searcher architecture is
- 5 disabled between synchronization sequence bursts. In a sample storage or asynchronous mode, portions of stored signals do not belong to any hypothesis to be tested (e.g. portions that occur between synchronization signal bursts) are not loaded into the searcher delay chain.

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